Subhradip Chakraborty

Email: 20ec3038@rgipt.ac.in
Mobile: +91-8240431059

LinkedIn: https://www.linkedin.com/in/subhradip-chakraborty
Github: https://github.com/subhradip096

Education

- **Rajiv Gandhi Institute of Petroleum Technology** — Jais, India
  Bachelor of Technology - Electronics Engineering; CGPA: 9.11 — *December 2020 - May 2024*
- **Don Bosco School Liluah** — Howrah, India
  Indian School Certificate Examination (ISC); Percentage: 95% — *June 2018 - May 2022*
- **Don Bosco School Liluah** — Howrah, India
  Indian Certificate of Secondary Education Examination (ICSE); Percentage: 91% — *January 2007 - May 2018*

Technical Skills

- **Languages**: Python, C, C++
- **Hardware Description Languages**: Verilog, System Verilog, UVM (Basic), VHDL (Basic)
- **EDA Tools**: Xilinx Vivado, Xilinx ISE Design, OrCAD PSpice, OrCAD Allegro, eSim
- **Libraries**: Turicreate, Numpy, Pandas, Scikit
- **IDE**: MATLAB, Arduino

Internships

- **Defence Research and Development Organisation**
  Summer Trainee — *May 2022 - July 2022*
  - **Supervisor**: Dr. Raghvendra Sahai Saxena, Scientist-F, SSPL, Delhi
  - **CMOS Image Sensor**: Worked on the recent developments in CMOS Image Sensors. Studied various hardware implementation ways and recent developments of Machine Learning and Deep learning algorithms to implement low power CMOS Image Sensor devices. Also studied the design, architecture and various applications of CMOS Image Sensors.

Projects

- **Verilog Implementation of Microprocessor**: Ongoing
  - Currently designing the architecture of a **simple microprocessor** and **32-bit MIPS** processor with **RISC Instruction set architecture** having 5 pipeline stage. Planned on simulating it on **Xilinx Vivado** and implement it on **Xilinx FPGA** board.
- **SR Flip Flop to JK Flip Flop using Mixed Signal**: September 2022 - Ongoing
  - Conversion of SR Flip Flop to JK Flip Flop was implemented using **SKY130**. The SR Flip Flop was made of analog block using **Kicad and Ngspice** and the gates which provide input to the SR Flip Flop is made of digital block using **Verilog**. The whole design was simulated using open source software **eSim and SKY130**.
- **Communication Protocols in Verilog/System Verilog** : June 2022
  - Designed the **transmitter** and **receiver** units of inter-system communication protocols like **UART**, and designed the interface of **I2C** communication protocol for **EEPROM** in Verilog.
  - Simulated and tested the performance of the design in **Xilinx Vivado**.
- **IoT Based Weather Reporting and Prediction System**: May 2022
  - Designed the station to measure weather conditions using different kind of sensors to measure parameters such as **temperature** (DHT-11), **humidity** (DHT-11), **pressure** (BMP-180), **air quality index** (MQ-135, MQ-2) and **rainfall intensity** (Rain Sensor Module).
  - The sensors and the **wifi-module (NodeMcu)** was connected to the **Arduino Uno** to send the data in form of **json** files to the cloud **(ThingSpeak API)**. The data was recorded and displayed in the cloud. Used **Linear regression, KNN and SVM** model to predict temperature and condition of the sky (rainy, cloudy or clear).
- **Hospital Management System**: July 2021
  - Designed the program in **C language** using the concept of **files**, **arrays**, **string** and other basic programming concept.
  - The program had two sections one for **covid-19 vaccination** and the other for **covid-19 treatment**. The program was used to make a system record all the patient information and their current status along with a **detailed search feature** from the database. It was designed to be a portal which was accessed through login credentials to **add, edit, view patient information and check the status of every patient**.

Achievements

- Qualified **JEE Advanced (among the top 2%)** , JEE Mains and WBJEE.
- **Winner (Excellent Category)** of Mixed Signal SoC design Marathon organized by **FOSSEE, IIT Bombay**.
- Achieved a **Dept.Rank 3** overall in Department of Electronics Engineering, RGIPT.

Position Of Responsibility

- Vice-Chairperson at RGIPT-ACM Student Chapter.
- Teaching Volunteer at Gyanarpan Project Amethi. (Taught a batch of more than 100 students)
- Designing Head at IEEE-RGIPT Student Chapter.